

Remarks

Claims 1-15 are at issue. Claims 1-3, 7 and 9-11 stand rejected under 35 USC 103(a) as being unpatentable over Fielder (US 6,757,327). Claims 4-6, 8 and 12-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims.

General Comments

Fiedler is directed to recovering data in a serial data communication system and more particularly to “opening the eye of the incoming data stream”, See Col. 1, lines 54-59. The present invention is directed to minimizing the “trade between cycle time and clock-to-clock data valid time” in a clocking system for memory circuits. While both applications clearly deal with clocking systems, that is where the similarity ends. It is highly unlikely that these two diverse applications are solved in the same or similar ways and in fact the reality is that they are not solved in the same way or even a similar way.

Claim 1 requires an external clock. The examiner points to element 230 as the external clock, which is generated by a VCO (Voltage Controlled Oscillator). A VCO 228 is a recovered internal clock. The VCO 228 recovers the clock from the incoming data (See path 202, 207, 216, 224, 226). This is clearly not an external clock. Claim 1 is allowable.

Claim 1 requires an access clock. The examiner points to element 248. Elements 248A and 248B are parallel data paths (See Col. 5, lines 6-8). These are not clocks but the data being clocked. Claim 1 is allowable.

Claims 2-4 & 7 are allowable as being dependent upon an allowable base claim.

Claim 9 requires an access clock. The examiner points to element 248. Elements 248A and 248B are parallel data paths (See Col. 5, lines 6-8). These are not clocks but the data being clocked. Claim 9 is allowable.

Claim 9 requires delaying a clock line to form a master clock that is coupled to the master of a master and slave output register. The Examiner points to element 211A as the master clock and element 210A as the master. But element 210A is a latch not a master/slave output register. Claim 9 is allowable.

Claim 9 requires a third clock line to form the slave clock of the slave of the output register. The examiner points to 210B as the slave and 211B as the slave clock. But clearly 210B is not the slave of latch 210A but a parallel path of the data from equalizers 207A & 207B. Claim 9 is clearly allowable.

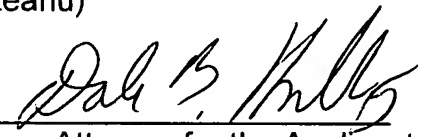
Claim 10 requires an external clock. The examiner points to element 230 as the external clock, which is generated by a VCO (Voltage Controlled Oscillator). . A VCO 228 is a recovered internal clock. The VCO 228 recovers the clock from the incoming data (See path 202, 207, 216, 224, 226). This is clearly not an external clock. Claim 10 is allowable.

Claim 11 is allowable as being dependent upon an allowable base claim.

Prompt reconsideration and allowance are respectfully requested.

Respectfully submitted,

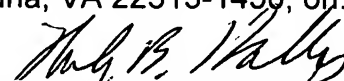
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